

Terry Fox & Associates

Serving the electronic design community with Signal Integrity and EMC training, consulting, an tool integration services since 1993.

JumpStart III Process by Terry Fox

www.SIEMC.com

DISCLAIMER....This is not a book. It is a summary of the JumpStart III process. It does not include answers to every situation, nor does this summary purport to cover all of the material in the class. It is just a summary. If you have taken the class this should make sense. Copyright 2007 All rights reserved. 6 pages total.

Triage Signals

Divide signals into three categories: Clocks, Busses, and Status

Clocks are signals with fast edges and a high repetition rate, but act alone

Busses are signals with fast edges and a high repetition rate, but act in parallel

Status signals are signals that do not switch very often and have no critical timing requirement.

Clock and Buss type signals will be analyzed rigorously.

Status type signals will be ignored. In the final steps of the process, we will perform a rigorous Cross Talk Analysis to make sure that Status signals do not become radiators as a result of coupling to Clock or Buss type signals.

Set Budgets for Clocks and Busses

Clock Type Signal Budgets

Clock must arrive at all receivers and pass monotonically through “low to high” or “high to low” switching region within X nS (pS).

Clock must have no more than X nS (pS) skew across all receivers.

Clock can have no more than X dbuV/M radiated emission. This number is typically 6 db below the applicable FCC or CISPR specification.

Clocks must have no more than X mV of over shoot or undershoot. Typically this is significantly less than one diode drop or about 707mV in silicon.

Clocks must not exceed X mA of drive current.

Clock signal may not deposit more than X mV of cross talk on a Buss signal during the setup and hold time.

Clock signal may not deposit more than X mV of cross talk on a Status Signal. This needs to be a very small number since cross talk can result in high EMI if coupled to a long status line.

Buss Type Signal Budgets

Buss signals must propagate and Ringing must settle within X mV at all receivers prior to the set up and hold timing window.

A Buss signal must have no more than X mV of cross talk induced from it's neighbors at any time within the set up and hold timing window.

Ground Bounce + Ringing + Cross Talk must remain above / below threshold switching voltage throughout the set up and hold timing window.

Buss, (assuming worst case average simultaneous switching), can have no more than X dbuV/M of radiated EMI. This is typically the FCC or CISPR specification – (6db + Simultaneous Switching Factor..ie 2 = 3db, 4 = 6db, 8 = 9db, etc.)

Individual Address or Data drivers must not exceed X mA of drive current.

All Buss signals collectively, (assuming worst case simultaneous switching), will draw no more than X mA of current on a single clock edge.

The power delivery system must provide this amount of current at an arbitrarily low impedance from DC to FMAX. $FMAX = ((1/RT)*5)$. If you can simulate EMI, FMAX can be precisely defined as the highest simulated EMI component that is less than 20 db below the FCC or CISPR design specification.

No Status signal may receive more than X mV of cross talk from a Buss signal. This needs to be a very small number since cross talk can result in high EMI if coupled to a long status line.

Select a Board Stack-up, Space, Trace, and Via Size

The board vendor must agree that this is a valid stack-up, trace width, space width, via size they can build for no uplift in price.

All simulations will be based on these dimensions. Get them right before you spend any significant time doing simulations. *A good starting stack-up is an 8 layer board. SH1, GND, SV1, VCC (for primary data buss I/O), GND, SH2, GND, SV2*

The stack-up must provide for high speed routing pairs of equal Z0 with a clearly defined return current path for all frequencies through FMAX.

Generally this means from DC to the microwave region.

Horizontal Vertical Routing Pairs on either side of a single unbroken ground plane are best because there is no possible ambiguity in the return current path.

Horizontal Vertical Routing Pairs referenced to two ground planes of the same voltage are second best because the return current path can be defined by one or more stitching vias between the ground planes.

Horizontal Vertical Routing Pairs referenced to planes of different voltages, ie VCC and GND are the most difficult because the return current path is through the capacitive array. This is a complex path from both a frequency and a physical distance stand point. If you choose this path, you must analyze the return current impedance at each and every signal via that switches between the planes. The impedance must be on the order of a few ohms from DC through FMAX. The capacitors must be within a very short distance of the signal via in order to avoid making large loops which will result in Common Mode EMI.

The stack-up must provide for a parallel plate capacitor to by pass any frequencies required or generated by any combination of drivers that can not be bypassed using a reasonable number of discrete capacitors.

This is normally the CPU to Memory Buss. (The alternative is to pray that there is enough on die capacitance to cover from the highest effective frequency of the capacitive array to FMAX.) Failing to accomplish this will result in a major Common Mode EMI conversion mechanism as well as a major Ground Bounce mechanism.

The Power Delivery Network impedance for the main processor to memory data buss must be in the range of 0.1 ohm from DC to the highest frequency of interest termed FMAX. A safe number can be calculated using the Power Impedance and Ground Bounce Calculator. This is an Excel spread sheet available on www.siemc.com. In all cases, the needs of the power delivery system are determined by the impulse current requirements. Worst case is a buss where all signals switch in the same direction at the same time. This can result in a current demand approaching 1 Amp or more in a sub nanosecond time frame..

FMAX (simple version) = [(1 / Rise Time) * 5] A precise FMAX can defined as the highest EMI frequency that is less than 20db below the relevant FCC or CISPR specification.

Perform Pre-Layout Simulation

Clock Lines

Establish topology, termination value, termination location, max current, max total length, and max length on the surface (*driven by EMI limits*) in order to meet the electrical budgets specified above.

Establish how close the Clock can be to a Status signal for some given distance and produce less than the budgeted amount of cross talk. This will be a table of lengths in parallel at various distances versus cross talk voltages.

Address Buss

Establish buss topology, termination value, termination location, max current, max length total, and max total length on the surface.

Establish how close the Address line can be to another Address line and produce less than the budgeted amount of cross talk on the quiescent Address line within the set up and hold window. This number must be adjusted for a worst case scenario where a quiescent Address line is in the middle of a number of other Address lines which are all switching in the same direction at the same time.

Establish how close the Address line can be to a Status signal for some distance and produce less than the budgeted amount of cross talk. This will be a table of lengths in parallel at various distances versus cross talk voltages. For practical purposes, you will probably pick a spacing and simulate for worst case cross talk. If the number is reasonable, put it into the budget and make sure all the numbers added together including Ringing and Ground bounce do not exceed the total noise budget.

Data Buss

Establish buss topology, termination value, termination location, max current, max length total, and *max length on the surface (this is driven by EMI)*.

Remember to run simulations from any possible driver on the buss.

Establish how close a Data line can be to another Data line and produce less than the budgeted amount of cross talk on the quiescent Data line within the set up and hold window. This number must be adjusted for a worst case scenario where a quiescent Data line is in the middle of a number of other Data lines which are all switching in the same direction at the same time. For practical purposes, you will probably pick a spacing and simulate for worst case cross talk. If the number is reasonable, put it into the budget. and make sure all the numbers together including Ringing and Ground bounce do not exceed the total noise budget.

Establish how close the Data line can be to a Status signal for some distance and produce less than the budgeted amount of cross talk. This will be a table of lengths in parallel at various distances versus cross talk voltages.

Design Main Power Delivery System

Generally this is the CPU to Memory driver supply. Do you have the correct number and type of capacitors? Are they connected properly using minimum inductance connections?

Power Ground Planes are 10 mils or closer

Are all the capacitors on the board?

Are there any “green spaces”?

Do all capacitors connect directly to the P/G planes?

Do all active devices connect directly to the P/G planes with minimum length connections?

Power Ground Planes are greater than 10 mils

The impedance at each power deliver pin must be specifically analyzed by taking both the value and the location into account. (Although the Power Impedance Calculator will give you some useful information for estimating this number, this is a nasty job, don't go here unless you have no choice.)

Design Remaining Power Delivery Systems

This is generally a much simpler task than the Main Power Delivery system because there is far less Delta I involved. For example the core of a processor requires quite a bit of current and the processor is operating at a high clock rate, but there is a relatively small Delta I. In general I just use the manufacturer's recommendations in these situations. Often this will entail small copper pours to facilitate capacitor connection. Do not carve up an important plane that serves as a return current path for a critical high speed signal.

Pre-Layout Design Review

Board Stack-up

The board stack up must be specified in terms of number of layers, the purpose of each layer, the spacing between layers, the target impedance at a target signal width for each of the routing layers, etc.

Signal Rules

Each Signal should have physical routing constraints that address every aspect of the routing topology, signal width, spacing, valid routing layers, layer transition requirements, termination value, termination location, max length on the surface, and max length total

Who Participates

Layout personnel must participate in the design review as applies to the layout rules and the reason for the rules.

Layout the Board

Typically high speed critical signals are laid out first. They have the priority for routing channels. Often this will result in difficult trade off issues. Therefore you must perform as built simulations as necessary to answer these questions during and immediately after the high speed signal layout.

Post Layout Simulation

Simulate each Clock and Buss type signal to verify they will perform within the budget as they are actually laid out.

Perform a rigorous cross talk simulation to find potential cross talk regions between Status signals and Clock or Buss type signals.

Any cross talk regions must be simulated in detail to assure that there is no significant energy will be coupled which can result in EMI.

Validate all high speed routing paths to assure a well defined and adequate return current path

These are the standard JumpStart III high speed routing rules regarding layer changes and return current path control.

Validate Main Power Delivery System

Generally this is the CPU to Memory driver supply. Do you have the correct number and type of capacitors? Are they connected properly?

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Place Appropriate Filters on all Off Board Leads

Each signal has a required bandwidth. An appropriate filter is one which will pass that band and block all others. This filter should be as close to the board edge as possible and not signals should be routed crossing the area between the filter and the actual cable connection point.

Post Layout / Pre - Fabrication Design Review

Are all of the items prior to this step completed? If they are, here are the final steps.

1. Place items on the various layers so it will be obvious from examining the finished board that the board was stacked up in the correct order.
2. Place test circuits either on the board itself or on a scrap area of the panel which can be used to validate the impedance of all transmission lines and basic cross talk geometries.
3. Talk personally to the board fabrication house and get a final assurance that the board will be built with the exact layer stack up that has been assumed in all of the simulations.

X and Y are numbers that must be determined by the system designer. One must have detailed circuit and device knowledge to arrive at a the appropriate numbers

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If you need changes for you particular company, please email me and I will try to accommodate you.

Feedback is always appreciated..TFox

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