

Signal Integrity/EMC Process Implementation (3 days)

Process Implementation includes all of the material in Pro Tune Up II, but it is covered in much greater detail. We work through an actual design in the same manner the instructor would on a standard consulting job. The goal is to produce a pre-layout design review document which specifies PCB Stack-Up, Power Deliver, and Routing / Spacing / Termination Rules for the key signal types. In addition we produce Signal Loading, Signal Timing, and Signal Noise Budgets which are the foundation of predicting Design or Manufacturing Margin. In public classes where we have a mix of companies, we use a canned system design example. In private classes where there are no confidentiality concerns, we encourage the student to use their own design. The culmination of the class is to perform a pre-layout peer design review as we would in an actual project.

The general technology types addressed are CMOS clocked parallel buss (SDRAM or DDR2), SERDES (PCI Express), differential LVDS, and mixed signal analogue digital boards.

To register for this class go to www.siemc.com and click on the Registration tab.

Who should attend this class?

Any **Electrical Engineer, CAD Layout Designer, or Engineering Manager** who wants to understand the details of this methodology as it applies to their specific design challenge. Pro Tune Up, the 1 day class, covers all of the topics, but the budgeting and design review area is covered at light speed. The focus of Pro Tune Up is the big picture and the best way to do things that are guaranteed to work even if the solution is slightly over kill. The Process Implementation class covers the Pro Tune Up material in much more detail and adds the analysis dimension of "how good is good enough?" Instead of simply finding a solution is guaranteed to work, we spend the extra time to analyze how well it will work. This provides the basis for generating design margin information and possibly removing components to arrive at a solution that is good enough, but no overly conservative. Process Implementation provides a running start on using this methodology on your specific project.

Topics specifically covered in class:

- 1. The Jump Start Budgeting and Design Review Process** This is the roadmap for success when designing complex high speed designs. The Jump Start process is a framework that defines certain critical questions which must be answered in order to assure design implementation success. We move out of the realm of black magic and secret knowledge into the concrete reality of budgets, design margin, and physics. Some structures are predictable. Other structures are not predictable. The wise engineer understands the difference and can explain the ramifications to cost conscious non-technical people. The Jump Start process is the framework upon which we hang everything else we do.

2. PCB Layer Stack-Up In the good old days we needed layers to provide enough space to route the design. That was it. Solve the routing problem and we were done. Using 2008 technology, PCB layers must control high frequency currents and provide the high frequency by-pass capacitance which we may not be able to get out of discrete devices. PCB layer stack-up is the foundation of any design. Every professional must understand how to analyze a board stack-up in light of the high frequency requirements of the system.

3. Fundamental High Speed Design Principles There are key high speed signal routing, spacing, and termination principles which can only be violated at your peril. Applying these principles must be second nature to any electrical or layout designer who wishes to be considered a professional in this field. Ignoring these principles can result data errors, race conditions, radiated emissions failure, manufacturing yield problems, warranty return rate problems, mysterious software bugs, and physical device failure.

4. Power Delivery Network Design Any modern design has multiple power requirements. Some power delivery networks are very easy to implement. Typical processor to memory power delivery networks must produce over an amp of current in sub nanosecond time. Failing to provide proper power delivery can result in Ground Bounce (which causes data errors) as well as radiated EMI.

5. Radiated Emission Sources Understanding the fundamental EMI generation process is critical for producing quiet designs. If you design products in plastic boxes with long leads, it is generally easier to make a design work than it is to make it quiet. Seemingly innocuous things like connector placement can be critical. If you understand what causes EMI, passing FCC & CISPR radiated emissions tests is relatively easy and predictable.

6. High Speed Signal Topology and Termination Whether it is the clock, the address buss, or a high speed strobe, all signals beyond a critical length will ring and radiate if they are not properly routed and terminated. Proper topology and termination will result in solid circuits which have predictable timing margin, high manufacturing yield, low warranty return rate, and will also behave in sane manner when taken to the lab for testing. Properly designed circuits can also be markedly less expensive to manufacture.

7. Cross Talk Cross talk can have two nasty ramifications. First it can add noise to the signal and cause data integrity or clock integrity issues. Less well know is that fact that it can couple on to other circuits and cause enough radiated EMI that the product will not pass FCC / CISPR tests.

8. Split Planes Splitting planes and creating moats around parts has caused a host of nasty problems. There are safe ways to split planes and there are insane ways to split planes. It is prudent to understand the difference.

9. Processor or FPGA to Memory Interface Typical memory interfaces are very demanding. We work through the design issues on 133MHz SDRAM, and 300MHz DDR2 as examples of this class of problem. These types of design have power delivery issues as well as difficult termination, cross talk, and loop timing challenges.

10. LVDS & SerDes Interconnects. For design examples we use common LVDS and PCI Express. We distinguish between the behavior of true differential and pseudo differential circuits. We discuss how these types of circuits work and what you need to do to produce predictable behavior.

11. Managing the Analogue Digital Interface We will discuss techniques for designing boards that have "noisy digital" on one side and "low level analog" on the other side. There are a number of plane splitting and layer isolation techniques which are very poor design practice and yield fairly marginal performance.

12. Connectors, Placement and Proper Signal Routing Whether it is a backplane or simply an I/O cable, there are key principals which must be observed for proper signal behavior.

13. Signal Timing, Loading, and Noise Margin's Adding up the numbers prior to the pre-layout design review results in predictable manufacturing margins and solid reliable products.

14. The Pre-Layout Design Review

15. Final Steps in the Process

This class is normally delivered as a private class and is often substituted for project consulting.

Tuition is \$2100 per seat for the public class and \$18,000 per class of 12 or less + T&L for the private on-site class.

More Questions? Please call or email :

**Terry Fox
Office 425 391-8696
Cell 425 785-2902
tfox@siemc.com
www.siemc.com**