

Terry Fox & Associates

Serving the electronic design community with Signal Integrity & EMC training, consulting, and tool integration services since 1993.

Pro Tune Up 4 for 2011

Target Audience: Engineers and CAD Layout Designers who must implement high speed digital and mixed analog digital systems that will work reliably at full speed and still remain quiet enough to pass regulatory EMI tests. The basic methodology upon which this class is based on a process which has been documented to achieve repeatable first pass success.

Content :

Basic Signal Integrity including board layer stack-up specification, high speed routing topology, space, trace, termination practices, and return current control. Get this wrong and the system will reward you with a host of problems including False Clock, False Data, Negative Timing Margins, Clock Jitter, Excessive EMI as well as a host of Manufacturing and Reliability issues.

Power Delivery is a lot more than one 0.1uF and five 0.01uF caps per pin. Power delivery depends upon stack-up, capacitor selection, placement, mounting technique, and quantity. Typical target impedance for memory systems must be around 0.1 ohm from DC to the highest frequency of interest. The highest frequency of interest is most likely in the microwave region. Poor design can result in power delivery impedance poles and inter plane resonances. Many of the mysterious SI and EMI issues can be traced directly to poor power delivery design.

Root causes and cures for EMI. The class's primary approach is to stop the noise at the source. If noise is eliminated at the source, you do not need to chase it around the board. The recent proliferation of ASIC's from hell has prompted us to add a section on shielding and filtering. If the problem is in the device, not the board, and you can not find a better behaved substitute for that device, your only choice is to shield and filter.

Single Ended Bus Issues If you have a memory or address bus with both high and low speed devices, do the high speed devices belong close to the processor with the low speed devices farther away, or vice versa? How do you terminate? What about option slots?

True Differential vs Psuedo Differential With the huge noise margin available using LVDS devices, you can use almost any interconnect scheme. However there can be other complications like Cross Talk and EMI if you do it incorrectly. True differential connections are quite different and you need to know the difference.

Giga Bit Serial / SERDES interface routing issues ...PCI Express We explain what is important and also debunk some of the popular myths about routing these types of interfaces.

The Analog / Digital Interface i.e. Isolation vs. Communication ...

To Moat or Not to Moat. Understanding the issues related to "quiet grounds."

Connectors, Board to Board SI, EMI, and Power Issues

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Chip Level Package Issues and how to defend against them.

Shielding / Filtering Theory for Enclosures, SW Power Supplies, and Renegade Chips

Critical elements in an effective high speed system design process. Simply performing a solid pre-layout design review and including the correct personnel can raise your first time odds of success to at least 65%. Performing a proper Post Layout review can raise that success rate to 90% even the first time you go through the process. A 99+% success rate is what you should expect after going through the process a couple of times.

Teaching Method: Explain, Demonstrate, Do

The instructor will **explain** the problem and an appropriate method to solve that problem.
The instructor will **demonstrate** the solution using industry standard software tools.
The students will **do** the work for themselves using lab computers and sample problems.

The students perform computer based labs to help lock in understanding of the physics behind classical high speed design problems. This also gives them the freedom to try their own examples. Simply hearing information results in about a 30% retention rate. Seeing a demonstration will raise the retention rate closer 50%. If you actually do the work on something meaningful to the student, the retention is over 80%.

The purpose of this class is not to impress anyone with complex formulae and higher math. There are perfectly good simulators to do the heavy lifting. The purpose is to give layout designers and EE's the tools to make their next design a quiet, reliable, full speed system on the first try.

Location & Tuition for Pro Tune Up 4

PTU4 is offered throughout North America as a public 1 day class which includes hands on labs using standard industrial simulations tools. Assuming registration 10 days in advance of class and payment 5 days in advance of the class, tuition is \$695. Late registration / payment is \$795. The schedule of classes is on: www.siemc.com/class_schedule.htm

Private On-Site Pro Tune Up 4 Classes

PTU4 is also offered as an onsite company private class for \$7000. This covers the tuition for up to 10 students. The price includes the instructor's T&L expenses and the computers used for the labs. Client is responsible for the meeting room, projector, and student lunches. Consulting days can be appended to PTU4 training in order to expand on the class material or to jump start a new project. Consulting days coincident with the class are \$3,500 per day including T&L.

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